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| **Date:** | November 22, 2005 | **Pages:** | 13 (including this sheet) |
| **From:** | David W. O'Brien | **Senders Phone No.:**<br>**Senders Fax No.:** | (512) 338-6300<br>(512) 338-6301 |

## *REGARDING:*

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|---|---|---|---|
| **Title:** | PIPELINED PROCESSOR WITH MULTI-CYCLE GROUPING FOR INSTRUCTION DISPATCH | | |
| **Application No.:** | 09/583,097 | **Filed:** | August 2, 1999 |
| **Examiner:** | Huisman, David J. | **Group Art Unit:** | 2183 |
| **Atty. Docket No.:** | 004-1391-1 | **Confirmation No.:** | 7166 |

**ATTACHED HERETO:**

(1) Reply Brief (37 C.F.R. § 41.41) (10 pages)
(2) Transmittal Letter (2 pages)

**CERTIFICATE OF FACSIMILE TRANSMISSION**

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David W. O'Brien — 22-Nov-05 (Date)

Respectfully submitted,

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November 22, 2005

Mail Stop Appeal Brief - Patents
Commissioner for Patents
P.O. Box 1450
Alexandria, VA 22313-1450

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| Applicant: | Marc Tremblay | | |
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| Examiner: | Huisman, David J. | Group Art Unit: | 2183 |
| Atty. Docket No.: | 004-1391-1 | Conf. No.: | 7166 |

Dear Sir:

Transmitted herewith are the following document(s) in the above-identified application:

(1) This Transmittal Letter (2 page(s))
(2) Reply Brief (37 C.F.R. § 41.41) (10 page(s))
(3) Return Postcard

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PATENT



IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

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22 November 2005

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# REPLY BRIEF (37 C.F.R. § 41.41)

This brief is in response to Examiner's Answer, mailed September 22, 2005, which sets a period for reply ending November 22, 2005. Applicants respectfully request consideration of the following in connection with the present appeal.

## REAL PARTY IN INTEREST

The real party in interest in this appeal remains Sun Microsystems, Inc., the assignee of record, as evidenced by the assignment recorded at Reel/Frame 008052/0437.

## RELATED APPEALS AND INTERFERENCES

Applicant is unaware of any prior or pending appeal, interference or judicial proceeding, which may be related to, directly affect or be directly affected by or have a bearing on the Board's decision in the pending appeal.

## STATUS OF CLAIMS

Claims 9-34 are pending and are finally rejected. Rejected claims 9-34 are the subject of this appeal.

## STATUS OF AMENDMENTS

An amendment was filed, 7 February 2005, subsequent to the final rejection. That amendment has been entered for purposes of appeal as indicated by the Advisory Action mailed 17 February 2005 and apparently disposes of various claim informalities objected to by the Examiner. A second after-final amendment accompanied the Appeal Brief. That second after-final amendment, which has also been entered, cancelled claims 35 and 36.

## SUMMARY OF CLAIMED SUBJECT MATTER

The summary of claimed subject matter contained in the Appeal Brief remains correct.

## ARGUMENT IN REPLY

Claims 9–34 were rejected under 35 U.S.C. 102(b) as being anticipated by Sites et al., U.S. Patent No. 5,193,167 (hereinafter *Sites*). In the final rejection the pending claims, the Office misinterpreted certain aspects of *Sites'* disclosure. In the Appeal Brief, Applicants identified five (5) significant errors of interpretation (which are summarized below):

(1) The Final Action apparently construes *Sites'* first four pipeline stages, i.e., fetch (S0), swap (S1), decode (S2) and register access/issue (S3) as "instruction grouping for dispatch, including both intra-group and inter-group dependency checking." *See* Final Action ¶12. In particular, the Office states that: "over multiple cycles (S0-S3) plus any stall cycles, dependencies and resource constraints are checked."

(2) Related to (1), the Office's analysis seems to suggest (and perhaps relies upon reasoning that) a pipeline stall acts to transform a single-cycle operation into a multiple-cycle operation. *See* Final Action ¶12.

(3) The Office further construes *Sites'* first two pipeline stages, i.e., fetch (S0) and swap (S1), as intra-group dependency checking that spans multiple cycles. *See* Final Action, ¶16. To be specific, the Office states in the Final Action that: "fetching is considered a portion of intra-group dependency checking because if instructions aren't fetched, then they cannot be checked for dependencies.

(4) Next, and perhaps fundamentally, the Office appears to assume that Sites' swap stage (S1) constitutes intra-group dependency checking. *See* Final Action throughout, but particularly ¶¶16, 17.

(5) Finally, with respect to claim language relating to evaluation of "non-deterministic conditions," the Office leverages a definition of "nondeterminism" (Final Action, ¶¶19, 23, 33, 34) in a way that is simply absurd and contrary to accepted meaning.

After review of the Examiner's Answer, it appears that the Office no longer relies on reasoning related to propositions (2) and (3) above, that parties simply disagree as to proposition (5) and that the Office's position now turns on the viability of proposition (4).[1] While the disavowal of the Office's prior reasoning with respect to propositions (2) and (3) is not totally unequivocal, the import of the Office's revised argument is clear and to the extent still necessary, the Appeal Brief covers Appellant's positions related thereto. Assuming that Appellant's arguments with respect to propositions (2) and (3) were, in effect, persuasive, proposition (4) is necessary to all current rejections.

*Request that Prosecution be Re-Opened in light of New Grounds for Rejection*

Before we address the correctness of the Office's present interpretation *Sites'* S1 pipeline stage, we note that primary issue in the present appeal, namely whether operation of *Sites'* S1 pipeline stage constitutes intra-group dependency checking within the meaning of Appellant's claims and disclosure, was presented explicitly for the first time in the Examiner's Answer. As a result, the present record is somewhat limited in documentary evidence as to proper interpretation by the term "intra-group dependency checking" by persons of skill in the art. Similarly, the present record is somewhat limited in documentary evidence as to proper interpretation of *Sites'* S1 pipeline stage, particularly in light of the inconsistencies identified in *Sites'* and summarized[2] in the Appeal Brief.

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[1] Note that while the Office's final rejection of dependent claims 13 and 14 seemed to suggest a which is expressly asserted (for the first time) in the Answer.

[2] In the Brief, Appellant's suggested that *Sites* should not be understood to enablingly disclose any intra-group dependency check at swap stage S1, noting that, while the Examiner chooses to rely on a portion of the statement, "The second stage S1 is the swap stage, during which the fetched instructions are evaluated by the circuit 25 to see if they can be issued at the same time," Sites, col. 10, lines 38-41, the weight of the description as a whole (including the express language of the relied upon statement) establishes that dual issue decision making is performed by circuit 25, which necessarily places such performance in stage S3, since circuit 25 follows decode logic (and associated stage S2) in the pipeline flow.

In short, the Office has ignored the clear statement(s) attributing dual issue decision making to circuit 25 (stage S3) in favor of one inconsistent (and arguably errant) statement that better supports its theory of anticipation. At best, *Sites* is non-enabling for the proposition asserted. At worst, *Sites* (properly construed) is inconsistent the proposition asserted.

Appellant's position, which has been briefed in the Appeal Brief is that dependency checking is a term understood by persons of skill in the art and does not encompass any swap performed by *Sites'* S1 pipeline stage. This Reply Brief further details that position; however, Appellants believe that additional documentary evidence could be useful to the Board and that the Office's new assertions. Accordingly, in light of the Office's reliance of what are, in effect, ***new grounds*** for rejection, Appellants respectfully request that prosecution be re-opened.

However, even if prosecution is not re-opened, Appellants believe (as argued herein) that the Office's interpretations are not supportable and rejections should be reversed by this Honorable Board.

*Dependency Checking*

The Office and Appellant's clearly disagree as to the proper interpretation of "dependency checking." The Office's position, now advanced in the Examiner's Answer, is apparently necessary to each appealed-from claim rejection. In particular, the Office's position, as now advanced, appears to be that some form of determination is made at *Sites'* S1 (swap) pipeline stage and since some pairs of instructions may not be issued simultaneously, the inability to issue one based necessarily implies a "dependency check." *See e.g.*, Examiner's Answer, (10) Response to Argument, pp. 16-17.

While the interpretation is superficially attractive, it does not survive closer analysis. *Sites* describes a dual-issue processor architecture in which some instructions are executable only by one (of two) execution units and others are executable only by the other (of two) execution units. *See Sites* col. 9, line 45-63 and col. 10, lines 38-41. Thus, inability to simultaneously issue one instruction with another is based on the fact that a first execution unit (but not the second) executes integer operate, floating point load/store and floating point branch instructions, while the second execution unit (but not the first) executes floating point operate, integer load/store, integer branch and JSR instructions. A simultaneous issue prohibition, in *Sites*, is therefore ***not based on any dependency between instructions***; rather it is based on whether each of two instructions can be executed by the execution unit to which they are slotted. For example, two integer load/store operations are necessarily prohibited from simultaneous issue in *Sites* and that prohibition is not based on any dependency between the instructions. Indeed, although the

disclosure of *Sites* on point is exceeding thin and somewhat contradictory, the "swap" stage would arguably be better understood by a person of ordinary skill as swapping instructions into the appropriate slot for the applicable execution unit.

In short, contrary to the Office's position expressed in the Examiner's Answer, a determination that of two instructions in a fetch group, one cannot be grouped with the other for simultaneous dispatch because the execution unit to which it would have to be routed does not support the operation type ***does not constitute*** an intra-group dependency check (i.e., dependency check between multiple instructions of a dispatch group).

Since *Sites'* S1 (swap) stage does not constitute "intra group dependency checking," each appealed from rejection (as now reformulated in the Examiner's answer) fails to identify an intra-group dependency check that, together with an inter-group dependency check, are performed over multiple cycles. All claims are allowable and a notice to that effect is respectfully requested.

*Fetch Group vs. Dispatch Group*

Related to above, the Office's argument with respect to *Sites'* S1 (swap) stage necessarily hinges on an interpretation of "group" that is inconsistent with applicant's claim language. To be clear, in addition to reading out the "dependency" from "dependency checking", the Office's position with *Sites'* S1 (swap) stage is based on interpretation of "intra-group" as "intra-fetch-group." *See* Examiner's Answer, (10) Response to Argument, p. 17 ("This checking qualifies as 'intra-group' checking because the check occurs among instructions in the fetched group.").

Applicant's claims clearly recite that the relevant group is a "dispatch group." For example:

- claim 9 ("... instruction grouping for dispatch, including both intra-group and inter-group dependency checking ..."),
- claim 17 ("... to select a group of instructions from a program sequence thereof for dispatch ..."),
- claim 26 ("groups of instructions for dispatch"),

- claim 31 ("method of grouping instructions for dispatch") and
- claim 35 ("means for grouping, over plural pipeline stages, instructions for dispatch …").

Thus, properly interpreted, the "group" to which "intra-group" and "inter-group" limitations refer is a dispatch group, i.e., a group of instructions that, subject to favorable resolution of the recited dependency checks and, in some claims, additionally recited resource allocation checks, may be dispatched together.

In stage S1, *Sites* "group" of two instructions is best characterized as a *fetch group*, not a dispatch group. Indeed, if the particular constituents of a fetch group are such that *Sites* architecture does not provide an execution pipe for both, the fetch group really results in two distinct dispatch groups (each with one instruction). Under no circumstances, successful dependency checks or otherwise, will *Sites* architecture issue the two fetch group instructions together. Accordingly, it is simply incorrect to construe the pair as a dispatch group.

Therefore, *Sites'* S1 (swap) stage does not perform a "dependency check" amongst instructions of a dispatch group and whatever *Sites'* S1 (swap) stage does do, it does not operate on a group that constitutes a dispatch group. Each of the independent claims is allowable for at least this reason as well.

*Fetch as a Component of Swap*

Appellants have detailed (in the Appeal Brief) errors in the Office's interpretation of Sites S0 (fetch) stage as a component of swap. Neither stage S1 (swap), nor stage S0 (fetch) constitute intra-group dependency checking. However, the further argument that fetch as a precursor to swap constitutes a two-cycle intra-group dependency checking is not sustainable. While the Office continues to espouse a contrary view in the Answer, the attention of the Board is directed to the points made in the Appeal Brief.

At least claims 13, 18 and 31 remain rejected based on this error. Withdrawal of the rejections is respectfully requested.

*Branch Prediction*

Regarding claim 15, Appellants respectfully suggest that the Office confuses a "predicted subsequent state" that is used in making data dependency and resource allocation checks with a actual subsequent state of a process that is executes code past a predicted taken branch. The two are not the same and the rejection should be withdrawn.

*S(t+τ)*

Regarding claims 17 et seq. Appellants respectfully suggest that the Office confuses

> grouping logic coupled to the functional units and pipelined to compute, over plural cycles, T, of the processor, a future state, S(t+T), of the processor based on a prior state, S(t), of the processor and based thereon to select a group of instructions from a program sequence thereof for dispatch to the functional units

i.e., computation by grouping logic of future processor states and use of such computed future state to shape dispatch decisions, with the succession of actual states that are necessarily encountered during operation of a processor. Nothing in *Sites* computes future states over plural cycles for use in dispatch decisions; rather *Sites* decision making occurs in stage S3 and is based on the actual state of the processor observed at that time. The fact that *Sites* processor would necessarily exhibit a sequence of states is beside the point.

*Non-Deterministic Conditions*

Appellants have detailed (in the Appeal Brief) errors in the Office's interpretation of limitations related to non-deterministic conditions. While the Office continues to espouse a contrary view in the Answer, the attention of the Board is directed to the points made in the Appeal Brief. Claims 16, 20, 21, 30, 33 and 34 are allowable at least for those reasons reasons as well.

espectfully suggest that the Office confuses a "predicted subsequent state" that is used in making data dependency and resource allocation checks with a actual subsequent state of a process that is executes code past a predicted taken branch.

## CONCLUSIONS

For the reasons outlined herein and in the Appellant's Brief, the present rejection of claims 9-34 should be reversed. Accordingly, Appellant respectfully requests that this Honorable Board do so and direct the present application to be issued.

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## EVIDENCE APPENDIX

There is no evidence submitted pursuant to 37 C.F.R. § 1.130, 1.131, or 1.132 or any other evidence entered by the examiner and relied upon by appellant in the appeal.

## RELATED APPEALS APPENDIX

There are no decisions rendered by a court or the Board in any proceeding identified above in the Related Appeals and Interferences section.